

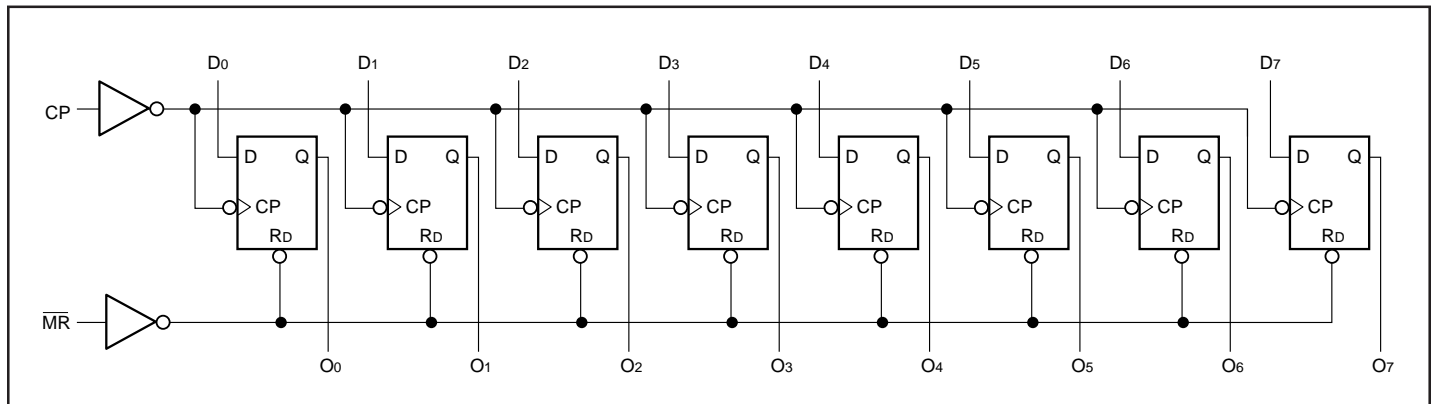
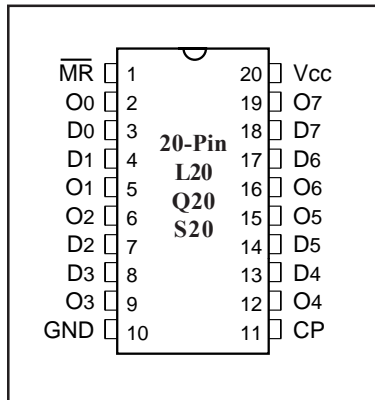
**Fast CMOS Octal D Flip-Flop
with Master Reset**
Features

- Pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to +85°C
- Packaging:
 - 20-pin 173-mil wide plastic TSSOP (L)
 - 20-pin 150-mil wide plastic QSOP (Q)
 - 20-pin 300-mil wide plastic SOIC (S)

Description

Pericom Semiconductor's PI74FCT273T is a 8-bit wide octal designed with eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{\text{MR}}$) load and resets (clear) all flip-flops simultaneously. The register is fully edge-triggered. The D input state, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{\text{MR}}$ input.

Device models available upon request.

Block Diagram

Pin Configuration

Pin Description

Pin Name	Description
$\overline{\text{MR}}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
D0-D7	Data Inputs
O0-O7	Data Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Mode	Inputs			Outputs
	$\overline{\text{MR}}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

1. H = High Voltage Level
 h = High Voltage Level one setup time prior to the LOW-to-HIGH Clock transition
 L = Low Voltage Level
 l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
 X = Don't Care
 ↑ = LOW-to-HIGH Clock Transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) ..	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -15.0mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 64mA		0.3	0.55	V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 12mA (25Ω Series)		0.3	0.50	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
IIH	Input HIGH Current	VCC = Max.	VIN = VCC			1	μA
IIL	Input LOW Current	VCC = Max.	VIN = GND			-1	μA
IOZH	High Impedance	VCC = MAX.	VOUT = 2.7V			1	μA
IOZL	Output Current		VOUT = 0.5V			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18mA			-0.7	-1.2	V
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V		—	—	100	μA
IOS	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-120		mA
VH	Input Hysteresis				200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	500	μA
ΔI _{CC}	Supply Current per per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open MR = V _{CC} , One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle MR = V _{CC} , 50% Duty Cycle One Bit toggling at f _i = 5 MHz	V _{IN} = V _{CC} V _{IN} = GND		1.5	3.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	3.5 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle MR = V _{CC} , 50% Duty Cycle Eight Bits toggling at f _i = 2.5 MHz, 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.8	7.3 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.0	16.3 ⁽⁵⁾	

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamperes and all frequencies are in megahertz.

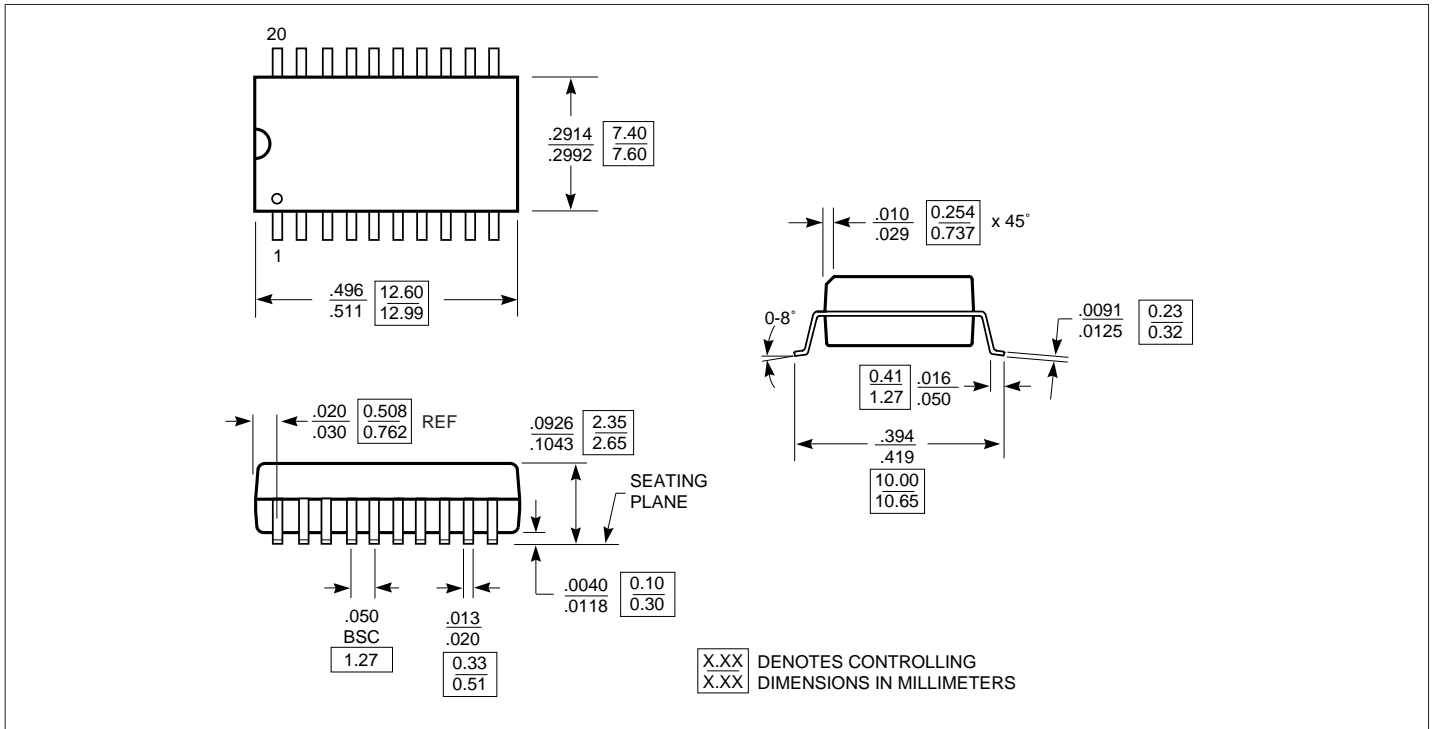
Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	273T/2273T		273AT/2273AT		273CT/2273CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay CP to ON	C _L = 50pF R _L = 500Ω	2.0	13.0	2.0	7.2	2.0	5.8	ns
t _{PHL}	Propagation Delay MR to ON		2.0	13.0	2.0	7.2	2.0	6.1	ns
t _{SU}	Setup Time, HIGH or LOW Dn to CP		3.0	—	2.0	—	2.0	—	ns
t _H	Hold Time, HIGH or LOW Dn to CP		2.0	—	1.5	—	1.5	—	ns
t _w	CP Pulse Width ⁽³⁾ HIGH or LOW		7.0	—	6.0	—	6.0	—	ns
t _w	MR Pulse Width ⁽³⁾ LOW		7.0	—	6.0	—	6.0	—	ns
t _{REM}	Recovery Time MR to CP ⁽³⁾		4.0	—	2.0	—	2.0	—	ns

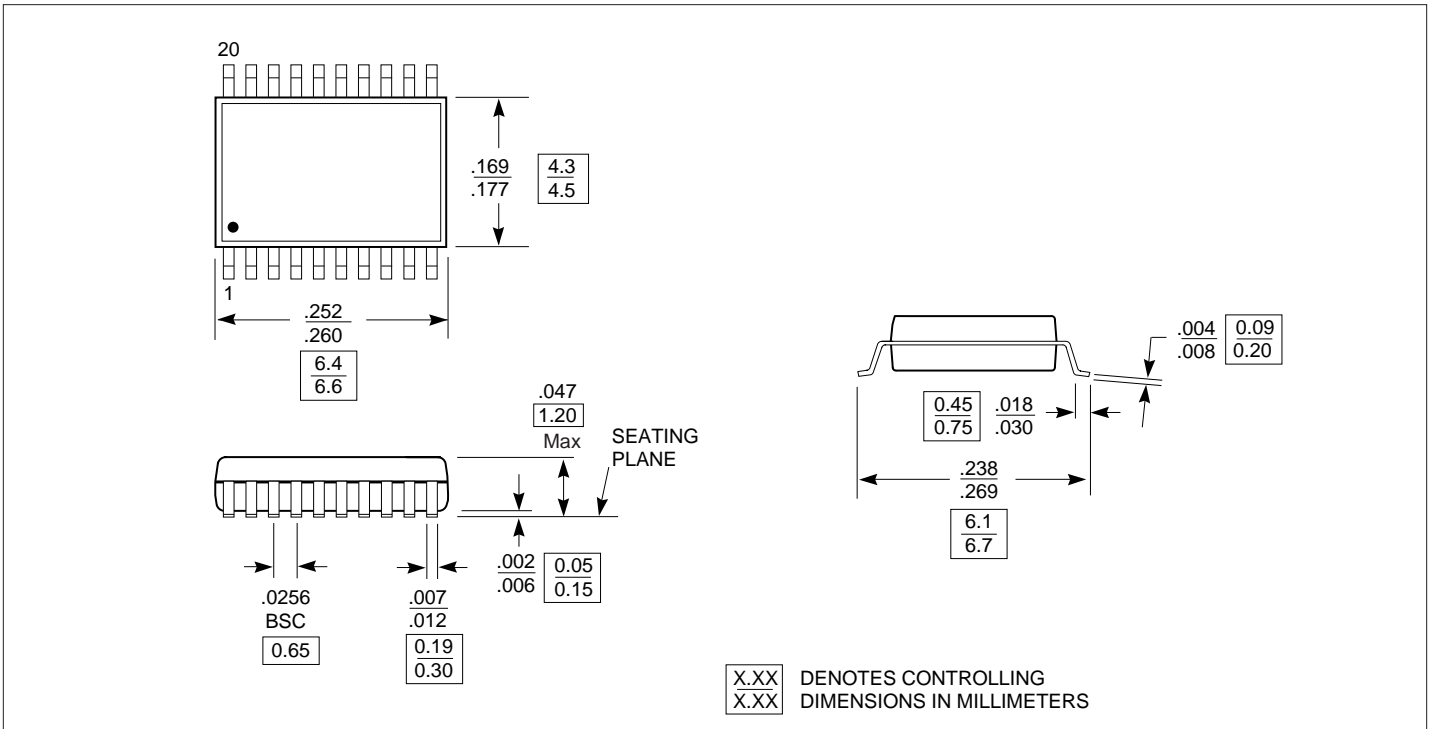
Notes:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not production tested.

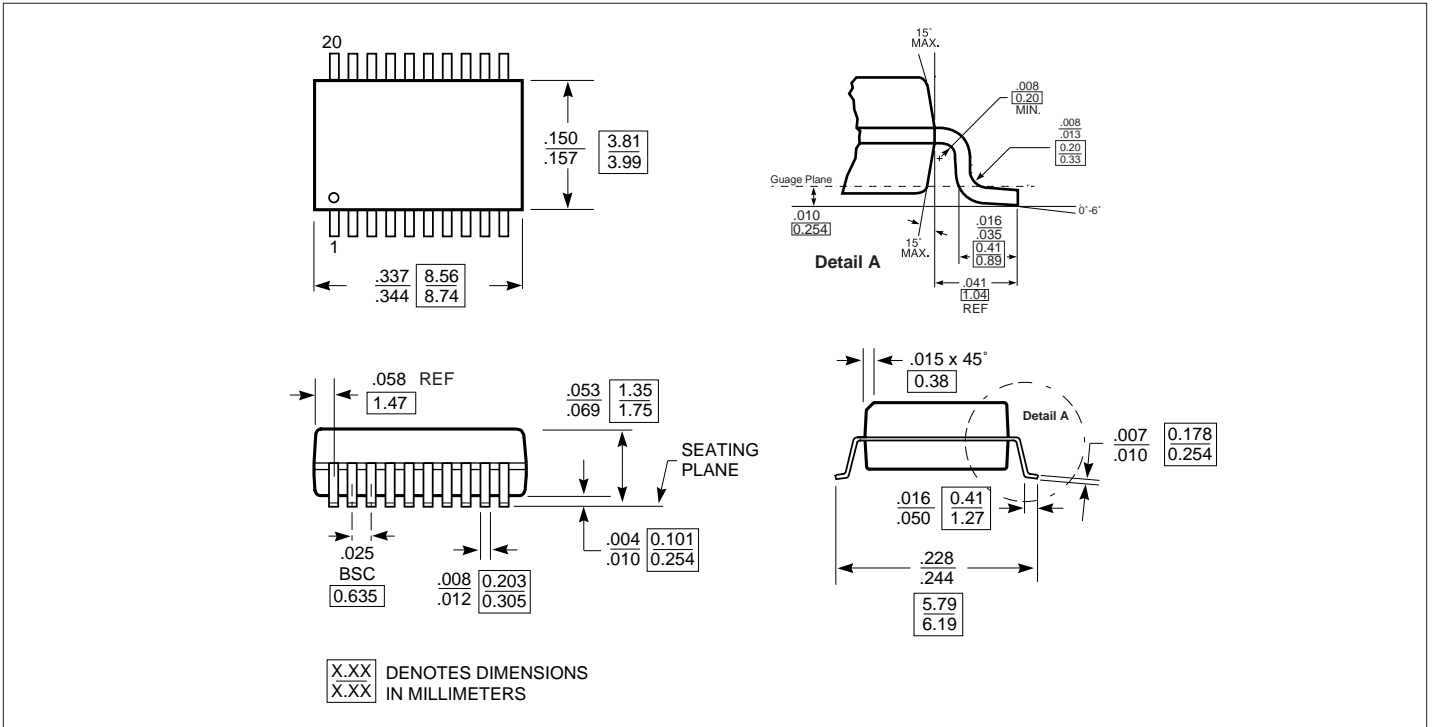
Packaging Mechanical: 20-pin SOIC (S)



Packaging Mechanical: 20-Pin TSSOP (L)



Packaging Mechanical: 20-pin QSOP (Q)



Ordering Information

Ordering Code	Package Code	Speed Grade	Package Type
PI74FCT273TQ	Q	Blank	20-pin QSOP
PI74FCT273TS	S	Blank	20-pin SOIC
PI74FCT273ATL	L	A	20-pin TSSOP
PI74FCT273ATS	S	A	20-pin SOIC
PI74FCT273ATQ	Q	A	20-pin QSOP
PI74FCT273CTL	L	C	20-pin TSSOP
PI74FCT273CTS	S	C	20-pin SOIC
PI74FCT273CTQ	Q	C	20-pin QSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/